ABSTRACT

[0066] A memory device with a low power control circuit that reduces power while ensuring that the device remains in a low power mode until a high power mode has been requested. The low power control circuit initially monitors a control signal using a CMOS buffer or inverter while a reference voltage is grounded or floated. Upon CMOS detection of a signal indicating that a high power mode is required, the low power control circuit monitors the signal using a differential amplifier and the specified reference voltage (i.e., ungrounded and un-floated reference voltage) to determine if the low power mode should be exited. In doing so, the low power control circuit prevents noise from inadvertently causing the device to exit the low power mode while at the same time reduces the power in the device.